## TCP® 9400 Etch



## System Reliability

- Uptime $\geq 88 \%$
- MTTC 12 hours
- MTBF $\geq 200$ hours
- MTBR $\leq 4$ hours


## Typical Results

- Poly ME Etch rate $\geq 2000 \mathrm{~A} / \mathrm{min}$
- Uniformity $+/-10 \% 3 \sigma$
- Selectivity poly to oxide (ME) $\geq 12: 1$
- Selectivity poly to oxide (OE) $\geq 125: 1$
- Profile control 88-90 degrees
- CD Bias $\leq \pm 0.03 \mu \mathrm{~m}$
- Particles $<0.06 / \mathrm{cm} 2$ at $>0.2 \mu \mathrm{~m}$ size

The TCP® 9400 system uses Lam's patented $\mathrm{TCP}{ }^{\circledR}$ technology and offers several key benefits for polysilicon etch.

The TCP® technology creates an inductively coupled, high-density plasma directly above the wafer while operating at low pressure.


Independent control of ion generation and ion energy allow etch processes to be optimized, providing excellent etch rates, profile control, and critical dimensions while ensuring minimal damage.

TCP® 9400 etch applications include :
PR mask over doped poly for $\geq 0.35 \mu \mathrm{~m}$ gate
UV PR and organic ARC mask over doped poly for $\geq 0.25 \mu \mathrm{~m}$ gate PR mask over undoped poly for $\geq 0.35 \mu \mathrm{~m}$ gate
DUV PR and organic ARC mask over undoped poly for $\geq 0.25 \mu \mathrm{~m}$ gate
PR mask over polycide ( $\mathrm{WSi}_{x} /$ poly) for $\geq 0.35 \mu \mathrm{~m}$ gate
DUV PR and organic ARC mask over polycide ( $\mathrm{WSi}_{x} /$ poly) for $\geq 0.25 \mu \mathrm{~m}$ gate


Coil
Dielectric plate
Wafer
Biased electrode


Hardmask gate (pre etched hardmask or in situ etch hard mask)
PR mask over nitride for $\geq 0.35 \mu \mathrm{~m}$ LOCOS

## WD6



